

CLAIMS

What is claimed is:

1. A method for testing a data recovery circuit, comprising:
disturbing a running variable in a closed control loop of a data recovery circuit (DRC) as the DRC is processing a received, test signal; and
evaluating data, wherein the data was recovered by the DRC while the DRC was affected by the disturbing.
2. The method of claim 1 wherein the disturbing comprises forcing a predetermined change to the value of a variable that represents a running phase of a phase interpolator loop of the DRC.
3. The method of claim 2 wherein the forcing the change comprises forcing a sampling phase register of the DRC to one of a) advance by a single count, and b) retard by a single count.
4. The method of claim 1 wherein the disturbing comprises:
forcing a sampling phase register of the DRC to advance, and then waiting for the DRC to compensate for the advance; and then forcing the register to retard.
5. The method of claim 1 wherein the evaluating comprises:
comparing a test data sequence with a sequence of said data recovered by the DRC.
6. The method of claim 1 wherein the disturbing and evaluating are performed as part of an integrated circuit design validation process.
7. The method of claim 1 wherein the disturbing and evaluating are performed as part of a high volume manufacturing screening process.
8. A method for testing a receiver, comprising:
disturbing a recovered clock phase of an oversampling receiver to simulate an effect of jitter in an input signal being processed by the receiver; and

determining robustness of the receiver using the disturbance.

9. The method of claim 8 wherein the determining comprises comparing a data stream, recovered by the receiver while under the influence of said disturbance, with a transmitted data stream.

10. The method of claim 8 wherein the disturbing comprises deterministically forcing a multi-bit binary variable that represents the recovered clock phase in a closed control loop of the receiver to change its value so as to simulate the effect of jitter in the input signal.

11. A method for testing a receiver, comprising:
injecting jitter, specified using a phase step magnitude and a frequency, into a running phase of a closed control loop in a data link receiver of an integrated circuit device; and
evaluating a data stream for an error, the data stream having been recovered by the receiver while the loop was affected by said jitter.

12. The method of claim 11 further comprising:
placing the integrated circuit device in a test mode of operation, prior to injecting jitter and evaluating the data stream, wherein the jitter injection is performed as part of the integrated circuit device's built in self test procedure.

13. The method of claim 12 further comprising:
programming one or more registers of the integrated circuit device with said magnitude and frequency; and
accessing one or more registers of the integrated circuit for a result of said evaluation.

14. The method of claim 13 further comprising:
looping back a clocked data stream, that was transmitted by the integrated circuit device, to said receiver to be recovered by the receiver while the loop is affected by said jitter.

15. The method of claim 11 further comprising:
determining a loop response of the closed control loop to said injected jitter.

16. The method of claim 15 wherein the loop response is determined by time stamping when the closed control loop has returned to within one phase step of the running phase at the time the jitter was injected.

17. An integrated circuit device comprising:

a chip I/O interface to a serial point to point data link, the interface having a receiver which includes an oversampling unit with an input for a received signal and an output for sampled data values, an advance/retard generator with an input for said sampled data values, a digital to analog converter (DAC) control unit with an input coupled to an output of the advance/retard generator, and an offset control unit with an input for a programmed test parameter and an output to force one of an advance and retard via the advance/retard generator.

18. The device of claim 17 further comprising:

a digital to analog converter (DAC) with an input coupled to an output of the DAC control unit; and

a mixer unit with an input coupled to an output of the DAC and an output to provide a sample clock to the oversampling unit.

19. The device of claim 17 further comprising:

a digital filter coupled between the advance/retard generator and the DAC control unit, an output of the filter coupled to the input of the DAC control unit.